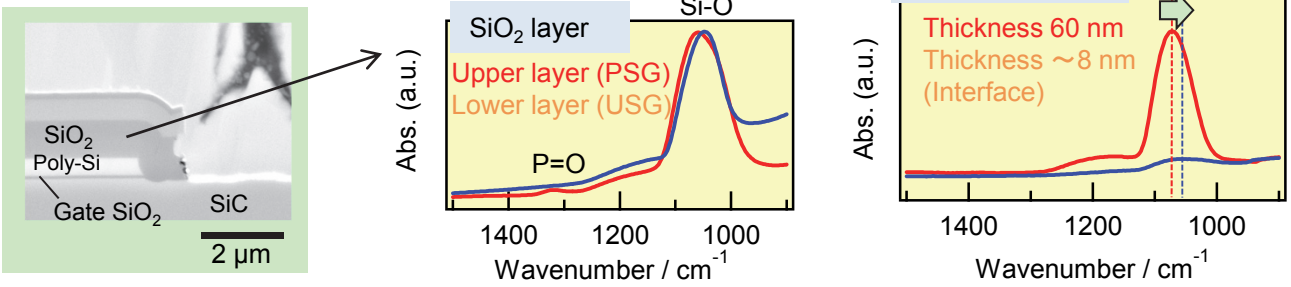
Characterization of stress, carrier concentration, and defects in SiC MOSFET

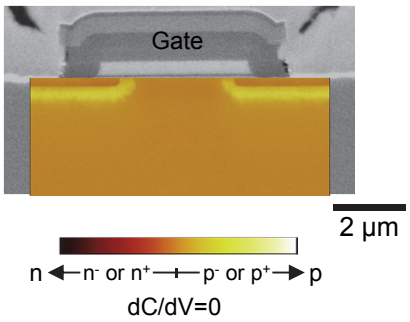
There are several issues about high-power SiC devices such as (1) reliability of gate oxide, (2) quality of SiC epitaxial film, (3) optimization of ion implantation, (4) packaging technology. These problems can be solved using scanning capacitance microscopy (SCM), cathodoluminescence (CL), Raman spectroscopy, and Fourier transform infrared spectroscopy (FT-IR).

Characterization of oxide film quality by FT-IR

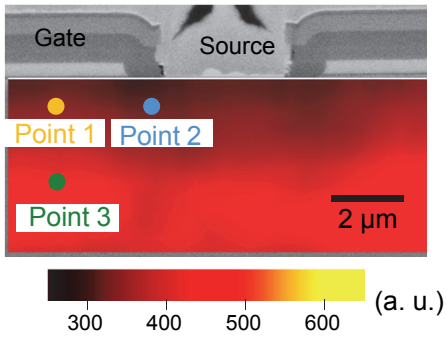


The quality of oxide films can be evaluated by FT-IR after decapping. The intermediate oxide film consists of PSG (phosphosilicate glass) and USG (undoped silicate glass). The peak wavenumber of gate oxide film is shifted near the interface. This indicates that the oxygen concentration decreases near the interface.

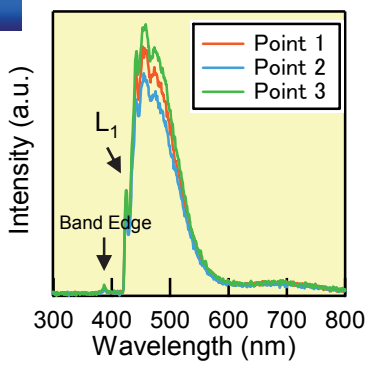
Characterization of carrier concentration and defects by SCM and CL



dC/dV image



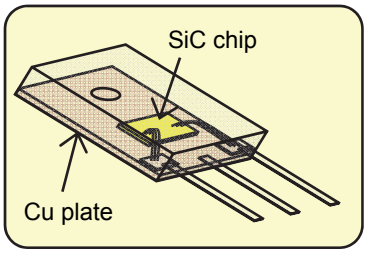
Monochromatic CL image of L_1 line

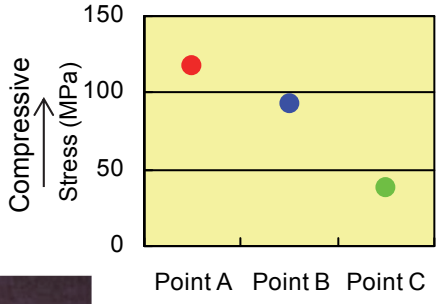


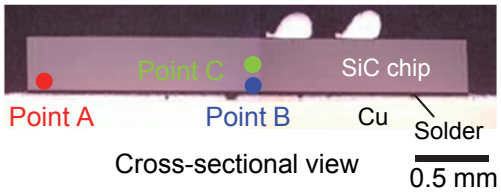
CL spectra

SCM can visualize the carrier distribution, while CL can evaluate crystalline defects in SiC MOFETs. The L1 line originates from the point defect whose structure is the anti-site pair of C and Si. The point defects generated by the ion implantation remains and diffuse into epitaxial layer entirely.

Stress evaluation by Raman spectroscopy

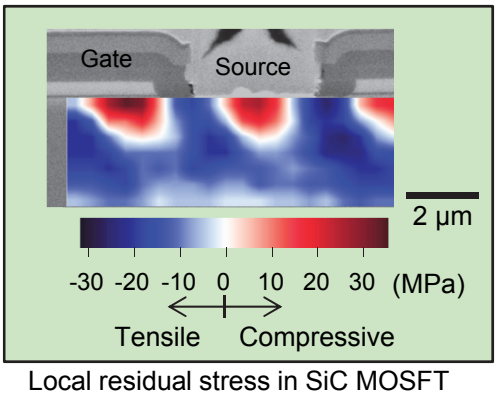






Cross-sectional view

0.5 mm



Local residual stress in SiC MOSFT

Stress in SiC devices can be evaluated by Raman spectroscopy. This device has the compressive stress up to 120 MPa near the interface between the chip and the solder.