

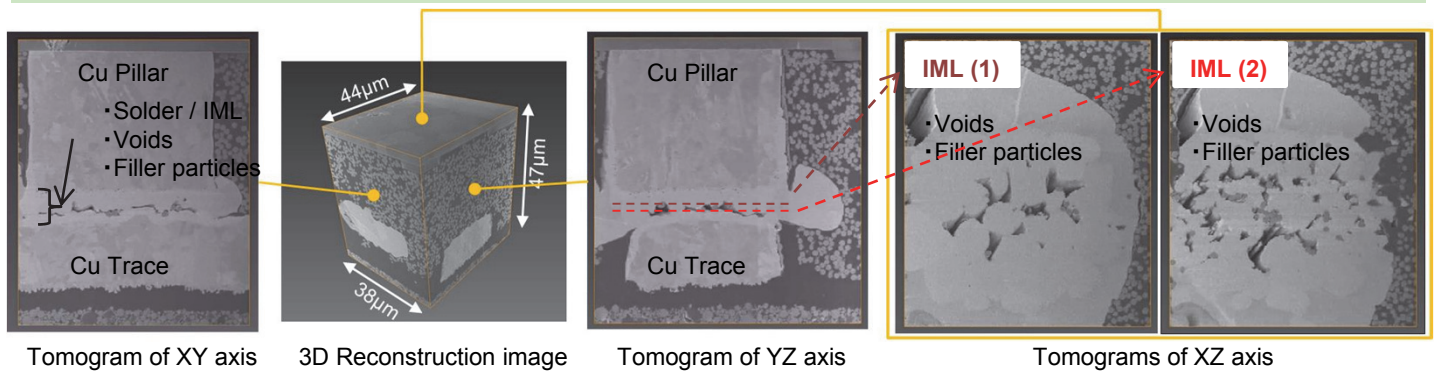
Evaluation of the Flip Chip Bonding

The flip chip joining technology has been performed a close-up of as internal wiring of the advanced LSI package. Three dimension of detailed observation of the junction was carried out by FIB-SEM. And the residual stress of Si die joined a flip chip to by Raman spectrometry was evaluated.

3D Reconstruction Images of Flip Chip Joint by FIB-SEM

(ICEP 2015 WB2-3 ; Kyoto, 04/15/2015)

Three dimensional SEM observation was performed for the flip chip bump interconnection analysis. It seemed that the interconnection was Cu pillar with solder cap bump and Cu trace on the substrate joint by thermal compression bonding process with pre-applied underfill resin. The three dimension view was made from 240 images which were taken by the repetition of FIB process and SEM observation at 200 nm pitch. This analysis revealed clearly that the joint had filler entrapment and a lot of void.

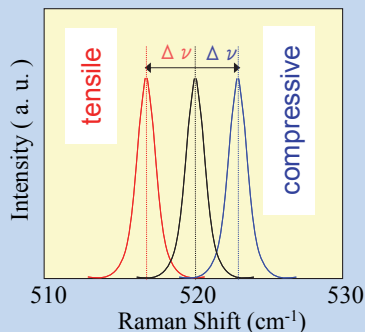


Evaluation of residual stress of flip chip Si die by Raman spectroscopy

(ECTC2015 s26p6 ; San Diego, 05/29/2015)

Non destructive Si die residual stress evaluation has been carried out by Raman spectroscopy. The measurement was implemented on the die backside. The dies were assembled on the 0.3 mm thick organic substrates by TCB with NCF. 12 mm x 12 mm size thickness dies, which were 50µm, were used. The corner of the die were investigated. Thick die sample evaluation results showed that the very corner end area had very low residual stress and 0.6 to 0.8 mm distant from the end showed compressive stress of 50 to 90 MPa at room temperature.

Raman shift by the stress of Si crystal



Frequency shift $\Delta\nu$ is proportional to the stress σ .

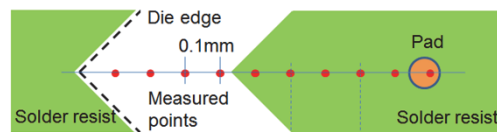


Fig.1 Layout of measured area

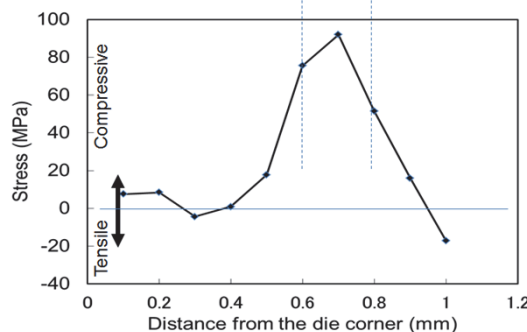


Fig.2 Stress evaluation results of die backside close to the corner by Raman spectroscopy.

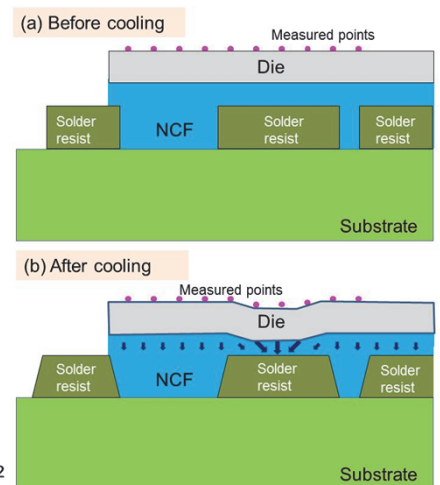


Fig.3 Cross-sectional schematic images.