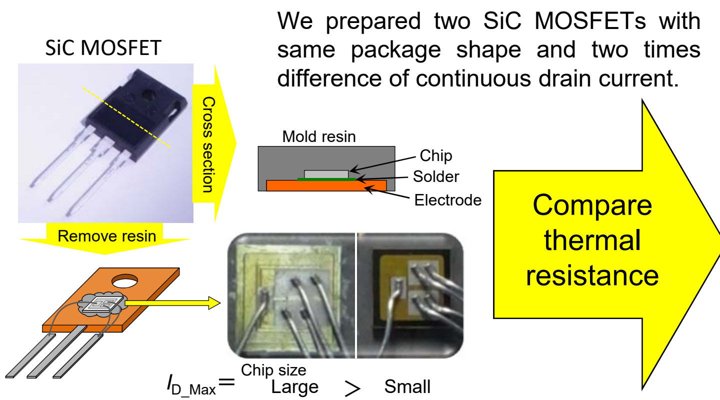
Failure Analysis of SiC Power Device Package

In failure analysis of semiconductor package, it is important to presume a failure part by nondestructive inspection method. For power devices generating a large amount of heat, it is effective to presume from the change in heat dissipation property before and after the failure. For example, a defect in the solder layer can be detected.

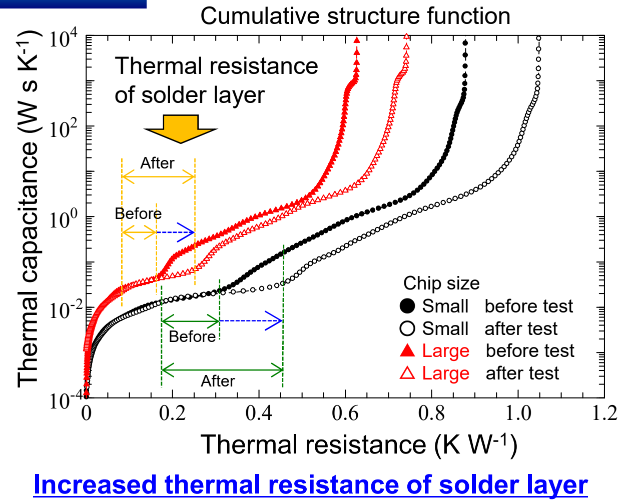
Presume the failure part by thermal transient measurement

We prepared two SiC MOSFETs with same package shape and two times difference of continuous drain current.



Compare thermal resistance

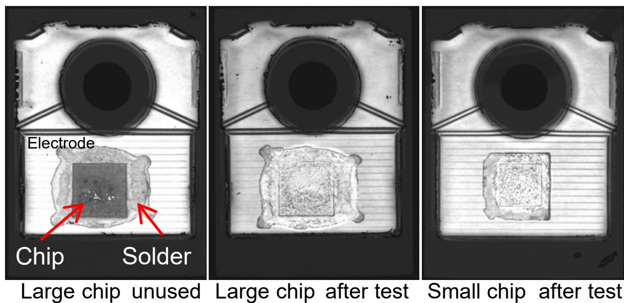
Confirm changes of thermal properties before and after heat shock test.



Increased thermal resistance of solder layer

Inspection by scanning acoustic microscopy

Scanning image measured from the backside of Cu electrode.



Large chip unused   Large chip after test   Small chip after test

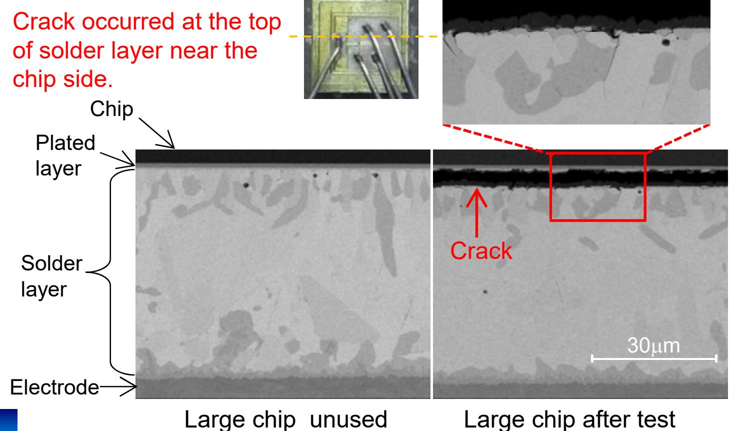
Around the chip after test looks white

→ It suggests the possibility of detachment occurred at the bottom of the chip.

Cross sectional image of solder layer

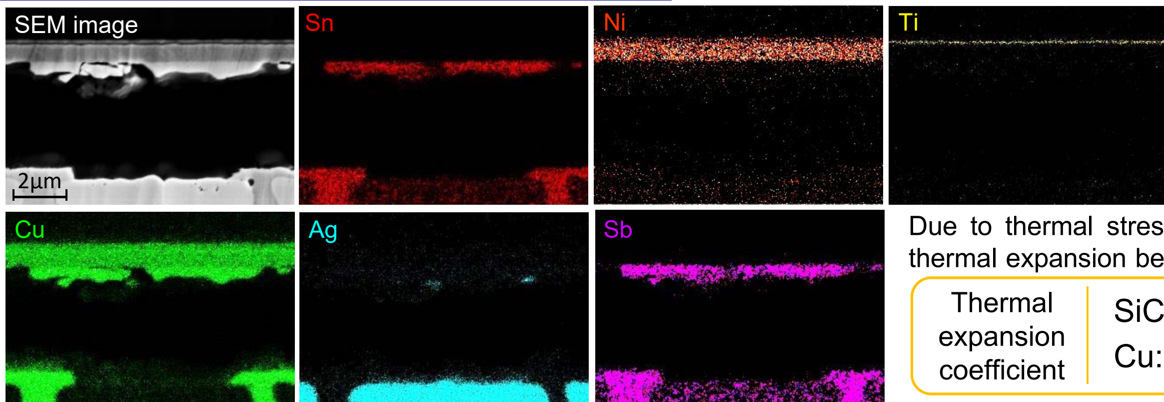
Cut the center of chip, and observed cross section by SEM.

Crack occurred at the top of solder layer near the chip side.



Large chip unused   Large chip after test

Elemental analysis around crack by SEM-EDX



Confirmed the separation at interface of Cu rich and Ag rich area.

Due to thermal stress by difference of thermal expansion between SiC and Cu.

Thermal expansion coefficient	SiC: 3.3×10^{-6} K^{-1} Cu: 16.7×10^{-6} K^{-1}

Ref.: Thermophysical properties handobook