Two-dimensional Raman mapping of stress in GaN HEMT packages from macro- to micro-scale

Stress management during semiconductor manufacturing is important in terms of its reliability since residual stress is typically caused by the local structure and packaging process. Examples of stress mapping in GaN HEMT packages are shown.

Stress mapping in Toray Research Center

Requirements for stress evaluation

- **High-accuracy measurement is necessary** because the peak shift of Raman line is typically small in most semiconductor packages.
- Conventional Raman imaging system has relatively low-accuracy, although it detects Raman signals sensitively.

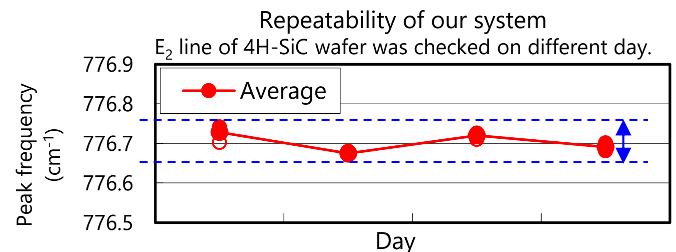
In Toray Research Center, measurement and analysis conditions can be optimized based on our wealth of experience. **Stress mapping data with high accuracy and resolution can be provided**.

Features of our stress mapping technique

- **Relatively large area up to 2 cm square can be evaluated.** The interval of measurement points becomes rough as the measurement area becomes wide.
- **Up to 10,000 points per one measurement** can be done.
- Wavenumber precision is **less than 0.05 cm^{-1}**. Frequency shift of 0.05 cm^{-1} corresponds to **15 MPa**.
- Semiconductor materials such as Si, SiC, GaN, Ga_2O_3, InP, GaAs, AlN can be evaluated.

Repeatability of our system

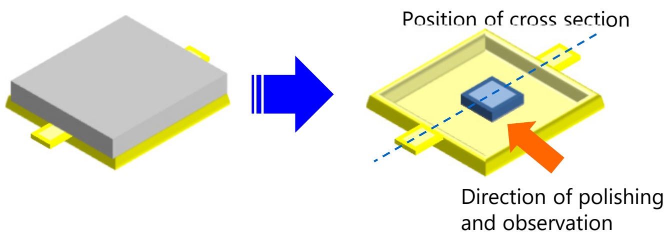
E_2 line of 4H-SiC wafer was checked on different day.



The peak frequency can be determined within 0.05 cm^{-1}(15 MPa).

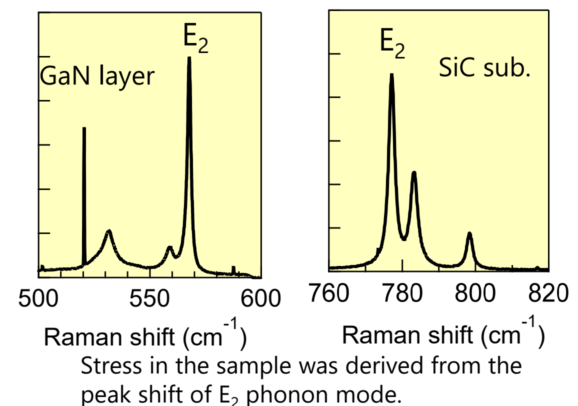
Examples of stress mapping

Sample：GaN HEMT discrete package（Commercially available）



The device was measured after the mechanical polishing.

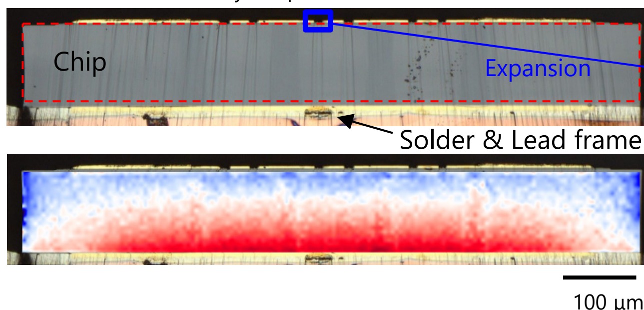
Examples of Raman spectra in the sample

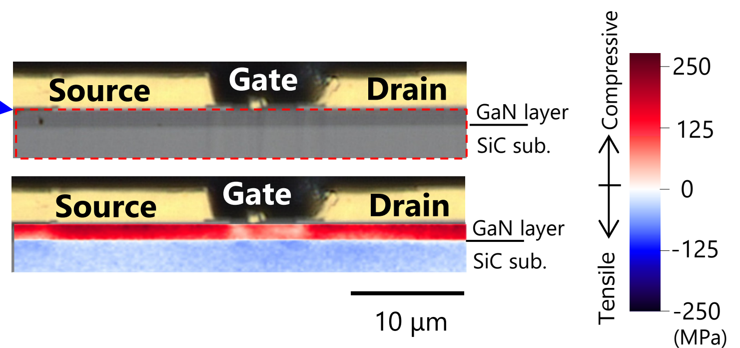


Stress in the sample was derived from the peak shift of E_2 phonon mode.

Stress distribution in whole area of GaN HEMT chip

Obtained by the peak shift of SiC substrate





Compressive stress was caused in the vicinity of solder and tensile stress was caused near the surface of the chip in SiC substrate.
⇒Compressive stress near the solder was generated because of the difference in coefficients of thermal expansion (CTEs) between the chip and solder after the solder reflow.

Stress in GaN layer was compressive and that in SiC substrate was tensile.
⇒ The stress difference was caused by the difference in CTEs between SiC and GaN during the heteroepitaxial growth.
Compressive stress in GaN layer was large under each electrode.
⇒ Electrodes affect the compressive stress in GaN layer.

Stress distribution in packaged devices can be visualized from macro- to micro-scale with high accuracy.
This technique can be used for stress distribution confirmation after the fabrication of devices and the verification of simulation results.

Toray Research Center, Inc.